PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Luo et al.

Serial No.: 10/826,985

Filed: April 19, 2004

For: METHODS FOR FORMING PROTECTIVE LAYERS ON SEMICONDUCTOR DEVICE COMPONENTS SO AS TO REDUCE OR ELIMINATE THE OCCURENCE OF DELAMINATION THEREOF AND CRACKING THEREIN

Confirmation No.: 3493

Examiner: J. Stark

Group Art Unit: 2823

Attorney Docket No.: 2269-5565.1US

VIA ELECTRONIC FILING
July 7, 2008

APPEAL BRIEF

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Commissioner for Patents
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Sirs:

This Appeal Brief is being submitted in the format required by 37 C.F.R. § 41.37(c)(1) and with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

U.S. Application Serial No. 10/826,985 (hereinafter "the '985 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel 013889, Frame 0234. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

There are currently no appeals, interferences, or other actions that are related to the '985 Application of which appellants or their attorneys are aware that may have a bearing on the outcome of the decision of the Board of Patent Appeals and Interferences in the above-referenced appeal.

(3) STATUS OF CLAIMS

There are currently twenty-eight (28) claims pending and under consideration in the '985 Application. No claims have been allowed.

The '985 Application was filed with twenty-nine (29) claims. Claim 24 was subsequently canceled. Claims 1-23 and 25-29 are currently pending and stand finally rejected in the above-referenced application. The final rejections of claims 1-23 and 25-29 are being appealed.

(4) STATUS OF AMENDMENTS

No claim amendments have been presented since the most recent final Office Action in the '985 Application was mailed on January 28, 2008.

On March 28, 2008, a Response to Final Office Action was filed. That Response was followed on April 15, 2008, by an Advisory Action. A Notice of Appeal, Pre-Appeal Brief Request for Review, and Preliminary Appeal Brief were filed on April 28, 2008.

The Examiner and other participants in the Panel for Pre-Appeal Brief Review elected to have Appellants to file a formal Appeal Brief in a Notice dated June 5, 2008. That Notice is followed by this Appeal Brief.

(5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 is drawn to a method for forming a protective layer on a plurality of semiconductor device components. The method of independent claim 1 includes, among other things, subjecting at least the protective material to conditions that will heal cracks and delaminated areas that were formed as the components were severed. *See, e.g.,* page 9, line 29, to page 10, line 20 (paragraphs **[0035]** and **[0036]**); page 11, line 20, to page 12, line 8 (paragraphs **[0041]** through **[0043]**; FIGs. 3-4A. After the protective material is subjected to such conditions, and *before* the resulting semiconductor device is assembled with another component of an electronic device, the protective material is fully cured. *See, e.g.,* page 11, line 4, to page 12, line 20; FIGs. 4 and 4A.

Claim 8, which depends from claims 5 and 1, recites that when the protective material is applied, it is spaced apart from a base portion of at least one conductive structure.

See, e.g., FIG. 10; page 15, line 9, to page 16, line 22 (paragraphs **[0058]** through **[0063]**). Dependent claim 25 recites that after the material of a protective layer on semiconductor devices carried by a fabrication substrate has been singulated, the semiconductor devices may be singulated from the fabrication substrate and the material of the protective layer may then be fully cured. *See, e.g.,* page 12, line 24, to page 14, line 27 (paragraphs **[0045]** through **[0055]**); FIGs. 5-8. Dependent claim 28 recites that regions of a protective layer that comprises thermoplastic material and that is located over at least a portion of a periphery of a semiconductor device may be healed after adjacent semiconductor components have been severed. *See, e.g.,* page 11, lines 21-26 (paragraph **[0041]**); FIG. 4.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 103(a) rejections of independent claim 1 and its dependent claims 2-8, 19-23, and 25-29 (claim 24 was previously canceled without prejudice or disclaimer) for reciting subject matter that is allegedly anticipated by the subject matter described in U.S. Patent Application Publication 2003/0171456 of Tong et al. (hereinafter "Tong"); and

(B) The 35 U.S.C. § 103(a) rejections of claims 9-18, which depend from independent claim 1, for being drawn to subject matter which is assertedly unpatentable over the teachings of Tong, in view of teachings from U.S. Patent 6,650,019 to Glenn et al. (hereinafter "Glenn").

(7) ARGUMENT

(A) APPLICABLE LAW

There are several requirements in establishing a *prima facie* case of obviousness against the claims of a patent application. All of the limitations of the claim must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Even then, a claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1396 (2007). The Office must also establish that one of ordinary skill in the art would have had a reasonable expectation of success that the purported modification or combination of reference teachings would have been successful. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). There must also be "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR* at 1396. That reason must be found in the prior art, common knowledge, or derived from the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006). A mere conclusory statement that one of ordinary skill in the art would have been motivated to combine or modify reference teachings will not suffice. *KSR* at 1396.

(B) ART RELIED UPON

Tong

Tong teaches that the B-stageable material is formulated so as to have a glass transition temperature that allows it to be "cleanly diced" once the material has been B-staged; *i.e.,* that *the material will not* stick to the dicing saw or *crack or break when sawed*. Paragraph **[0033]**. In the process of Tong, a B-stageable material is applied to a semiconductor wafer (*see, e.g.,* paragraph **[0013]**), the B-stageable material is partially cured by removing solvent therefrom (*see, e.g.,* paragraph **[0013]**), the partially cured material and the wafer are diced (*see, e.g.,* paragraph **[0013]**), and a semiconductor device that has been coated with the partially cured B-stageable material is assembled face-down over a substrate before the B-stageable material is fully cured (paragraphs **[0025]** and **[0026]**).

Glenn

The Examiner has relied upon Glenn's teaching of a preformed spacer 50 that includes a fiberglass matrix impregnated with a B-stage resin. Col. 8, lines 36-38. Additional adhesive layers 52 and 54 coat opposite surfaces of the spacer 50. Col. 8, lines 40-52. The spacer 50 is configured to separate the active surface of one semiconductor device 14 from the back side of another semiconductor device 16. Col. 7, line 61, to col. 8, line 35; FIG. 7.

(C) ANALYSIS

(1) TONG

It is respectfully submitted that, in the final rejections of the claims of the above-referenced application, a *prima facie* case of obviousness has not been established because Tong does not teach or suggest each and every element of independent claim 1. In the process of Tong, a B-stageable material is applied to a semiconductor wafer (*see, e.g.,* paragraph **[0013]**), the B-stageable material is partially cured by removing solvent therefrom (*see, e.g.,* paragraph **[0013]**), the partially cured material and the wafer are diced (*see, e.g.,* paragraph **[0013]**), and a semiconductor device that has been coated with the partially cured B-stageable material is assembled face-down over a substrate before the B-stageable material is fully cured (paragraphs **[0025]** and **[0026]**). Tong does not provide any teaching or suggestion that the B-stageable material may be subjected to conditions that will heal cracks and delaminated areas thereof, particularly ***before*** *the semiconductor device is assembled with another component* of an electronic device.

Furthermore, Tong teaches that the B-stageable material is formulated so as to have a glass transition temperature that allows it to be "cleanly diced" once the material has been B-staged; *i.e.,* that *the material will not* stick to the dicing saw or *crack or break when sawed.* Paragraph **[0033]**. Based on this teaching by Tong, there would be no apparent reason for one of ordinary skill in the art to believe that there is any reason to heal cracks or delaminations of the "cleanly diced" B-staged material of Tong. Nor does Tong provide any teaching or suggestion in this regard.

Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 1 is allowable over the teachings and suggestions of Tong.

Each of claims 2-8, 19-23, and 25-29 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 8, which also depends from claim 5, is further allowable since Tong lacks any teaching or suggestion of applying the protective material such that the protective material is spaced apart from a base portion of at least one conductive structure.

Claim 25 is additionally allowable because Tong neither teaches nor suggests singulating semiconductor devices from a fabrication substrate once the material of a protective layer on the semiconductor devices has been singulated, then fully cured.

Claim 28 is further allowable because Tong includes no teaching or suggestion of healing the protective material by heating at least portions of a *thermoplastic material* located over peripheral regions of the adjacent semiconductor device components following severing and at least partially severing.

(2) TONG IN VIEW OF GLENN

Each of claims 9-18 is allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

Claims 9-18 are further allowable because there would have been no apparent reason for one of ordinary skill in the art to combine teachings from Tong and Glenn in the manner that has been asserted. Specifically, there would be no apparent reason for one or ordinary skill in the art to use the sandwich-type spacer of Glenn, which includes fiberglass impregnated with a

B-stageable resin and sandwiched between two additional adhesive layers, in place of the simpler spreadable B-stageable material of Tong. Furthermore, one of ordinary skill in the art would have no reason to expect that the preformed sandwich-type spacer 50 of Glenn could be singulated in the manner required by Tong—where one of ordinary skill in the art would that the different material layers of that sandwich-type spacer would introduce a significant degree of difficulty into the dicing process.

For these reasons, it appears that one of ordinary skill in the art wouldn't have been motivated to combined teachings from Tong and Glenn in the asserted manner without the benefit of hindsight provided by the claims and disclosure of the above-referenced application.

Therefore, is respectfully submitted that the asserted combination of teachings from Tong and Glenn does not support a *prima facie* case of obviousness against any of claims 9-18 of the above-referenced application.

8. CLAIMS APPENDIX

The current status of each claim that has been introduced into the '985 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

9. EVIDENCE APPENDIX

There is no EVIDENCE APPENDIX to this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

There is no RELATED PROCEEDINGS APPENDIX to this Appeal Brief.

11. CONCLUSION

It is respectfully submitted that:

(A) Claims 1-8, 19-23, and 25-29 are drawn to subject matter that, under 35 U.S.C. 103(a), is allowable over the subject matter taught by Tong; and

(B) Claims 9-18 are each directed to subject matter that, under 35 U.S.C. § 103(a), is allowable over the teachings of Tong, in view of teachings from Glenn.

Accordingly, reversal of the 35 U.S.C. § 103(a) rejections of each of claims 1-23 and 25-29 is respectfully solicited, as is the allowance of these claims.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method for forming a protective layer on a plurality of semiconductor device components, comprising:

providing a fabrication substrate carrying a plurality of semiconductor device components, adjacent semiconductor device components on the fabrication substrate being separated from one another by a street extending therebetween;

applying a protective material to active surfaces of at least the adjacent semiconductor device components;

severing the protective material and at least partially severing the adjacent semiconductor device components from one another along the street;

subjecting at least the protective material to conditions in which cracks and delaminated areas in the protective material that were formed during the at least partially severing are healed; and

fully curing the protective material after cracks and delaminated areas are healed and before assembling a semiconductor device components of the adjacent semiconductor device components to another component of an electronic device.

2. The method of claim 1, wherein providing comprises providing a fabrication substrate with at least one bond pad exposed at an active surface of each of the adjacent semiconductor device components.

3. The method of claim 2, wherein providing comprises providing a fabrication substrate with a plurality of semiconductor device components comprising at least one of semiconductor devices, interposers, and carrier substrates.

4. The method of claim 2, wherein applying comprises applying the protective material such that the at least one bond pad of each of the plurality of semiconductor device components is exposed through the protective material sufficiently to effect electrical contact therewith.

5. The method of claim 2, wherein providing comprises providing the fabrication substrate with each of the plurality of semiconductor device components having a conductive structure protruding from the at least one bond pad thereof.

6. The method of claim 5, wherein applying comprises applying the protective material such that the protective material contacts a base portion of at least one conductive structure.

7. The method of claim 6, wherein applying comprises forming a support structure around the base portion of the at least one conductive structure.

8. The method of claim 5, wherein applying comprises applying the protective material such that the protective material is spaced apart from a base portion of at least one conductive structure.

9. The method of claim 1, wherein applying comprises applying a preformed sheet of protective material to the active surfaces.

10. The method of claim 9, wherein applying the preformed sheet comprises applying a preformed sheet comprising partially cured protective material.

11. The method of claim 9, wherein applying the preformed sheet comprises applying a preformed sheet comprising thermoplastic material.

12. The method of claim 9, wherein applying preformed sheet comprises applying a preformed sheet including apertures positioned to align with the at least one bond pad of each of the adjacent semiconductor device components.

13. The method of claim 2, wherein applying comprises applying a preformed sheet of protective material to the active surfaces.

14. The method of claim 13, wherein applying the preformed sheet comprises applying a preformed sheet comprising partially cured protective material.

15. The method of claim 13, wherein applying the preformed sheet comprises applying a preformed sheet comprising thermoplastic material.

16. The method of claim 13, wherein applying the preformed sheet comprises applying a preformed sheet including apertures therein positioned to align with the at least one bond pad of each of the adjacent semiconductor device components.

17. The method of claim 13, wherein applying the preformed sheet comprises applying the preformed sheet such that a conductive structure protruding from each of the adjacent semiconductor device components on the fabrication substrate passes through a plane of the preformed sheet.

18. The method of claim 17, further comprising heating each conductive structure prior to applying the preformed sheet.

19. The method of claim 1, wherein applying comprises applying the protective material in a liquid state.

20. The method of claim 19, further comprising spreading the protective material to form a protective layer on the active surfaces.

21. The method of claim 20, wherein applying the protective material in the liquid state comprises applying a quantity of a substantially uncured polymer to the active surfaces.

22. The method of claim 21, further comprising partially curing the polymer prior to severing and at least partially severing.

23. The method of claim 22, wherein subjecting is effected while the polymer remains in a partially cured state.

25. The method of claim 1, further comprising:

completely severing the adjacent semiconductor device components from one another along the street after fully curing the protective material.

26. The method of claim 20, wherein applying the protective material in the liquid state comprises applying liquefied thermoplastic material to the active surfaces.

27. The method of claim 26, further comprising permitting or causing the thermoplastic material to at least partially harden prior to severing and at least partially severing.

28. The method of claim 26, wherein subjecting comprises heating at least portions of the thermoplastic material located over peripheral regions of the adjacent semiconductor device components following severing and at least partially severing.

29. The method of claim 27, further comprising completely severing the adjacent semiconductor device components from one another along the street after subjecting at least the protective material to conditions in which cracks and delaminated areas in the protective material that were formed during the at least partially severing are healed.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE